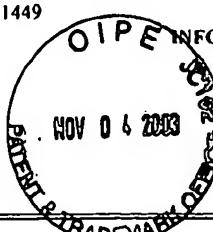
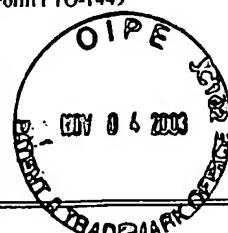


Form PTO-1449  (Use several sheets if necessary)				Docket Number (Optional) 068758.0102	Application Number 09/786,022 10/633,044	
				Applicant Deboy et al.		
				Filing Date 04/22/99	Group Art Unit: Group Art Unit:	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
P	3,171,068	02/23/65	Denkewalter et al.	317	234	10/19/60
	3,925,803	12/09/75	Kobayashi	357	22	07/12/73
	3,961,356	06/01/76	Okuhura et al.	357	50	10/31/74
	4,003,072	01/11/77	Matsushita et al.	357	52	11/01/74
	4,055,884	11/01/77	Jambotkar	29	571	12/13/76
	4,072,975	02/07/78	Ishtiani	357	23	04/22/77
	4,101,922	07/18/78	Tihanyi	357	23	03/09/77
	4,145,700	03/20/79	Jambotkar	357	23	08/08/77
	4,320,410	03/16/82	Nishizawa et al.	357	43	05/03/79
	4,345,265	08/17/82	Blanchard	357	23	04/14/80
	4,366,495	12/28/82	Goodman et al	357	23	08/06/79
	4,376,286	03/08/83	Lidow et al.	357	23	02/09/81
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation _____
	EP 0 053 854 B1	16.06.82	EPO	H01L	29/06	<input checked="" type="checkbox"/> NO
	GB 2 089 118 A	16.02.82	UK	H01L	29/78	<input checked="" type="checkbox"/>
	EP 0 069 429 A2	12.01.83	EPO	H01L	29/78	<input checked="" type="checkbox"/>
	EP 0 447 873 A2	01.04.92	EPO	H01L	29/784	<input checked="" type="checkbox"/>
	DE 43 09 764 A1	25.03.93	Germany	H01L	29/784	<input checked="" type="checkbox"/>
	DE 43 09 764 C2	29.9.94	Germany	H01L	29/78	<input checked="" type="checkbox"/>
<b>OTHER DOCUMENTS</b>						(Including Author, Title, Date, Pertinent Pages, Etc.)
		1967	A.S. Grove: "Physics and Technology of Semiconductor Devices" p 78-83			
		1976	B. Jayant Baliga, Sorab K. Ghandi: "Analytical Solutions for the Breakdown Voltage of Abrupt Cylindrical and Spherical Junctions" (p 739-744)			
		1977	Richard F. David: "Computerized Thermal Analysis of Hybrid Circuits" 27th Electronics Components Conference, May 16-18 1977 (p 324-332)			
EXAMINER <i>John R. Brehm</i>				DATE CONSIDERED 8/20/04		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						

Form PTO-1449  MAY 06 2003 EXAMINER TRADEMARKS SEARCHED	INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)	Doctc Number (Optional) 068758.0102	Application Number 09/786,022 10/633,044
		Applicant Debey et al.	
		Filing Date 04/22/99	Group Art Unit:

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE	
PB	4,404,575	09/13/83	Nishizawa	357	22	05/03/82	
	4,417,385	11/29/83	Temple	29	571	09/09/82	
	4,561,003	12/24/85	Tihanyi et al.	357	23.4	04/13/84	
	4,593,302	06/03/86	Lidow et al	357	23.4	08/18/80	
	4,748,103	05/31/88	Hollinger	430	314	03/21/66	
	4,754,310	06/28/88	Coe	357	13	12/04/84	
	4,775,881	10/04/88	Ploss et al	357	30	02/13/87	
	4,777,149	10/11/88	Tanabe et al.	437	142	12/22/87	
	4,895,810	01/23/90	Meyers et al.	431	41	05/17/88	
DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Trademarks		
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	EP 0 772 244 A1	07.05.97	EPO	HO1L	29/78	x	
	DE 196 04 043 A1	5.2.96	Germany	HO1L	29/78		x
	WO 97/29518	14.08.97	PCT	HO1L	29/78		x
	DE 196 04 044 A1	5.2.97	Germany	HO1L	29/78		x
	WO 97/35346	25.09.97	PCT	HO1L	29/78		x
	EP 0 834 926 A3	08.26.98	EPO	HO1L	29/08		x
	DE 197 30 759 C1	17.7.97	Germany	HO1L	29/78		x
	WO 99/04437	28.01.99	PCT	HO1L	29/78		x
	WO 99/23703	14.05.99	PCT	HO1L	29/06		x
	DE 198 08 348 C1	27.2.98	Germany	HO1L	29/78		x

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	IEEE	1977	Vinson C. Alwin, David H. Navon, Luke J. Turgeon: "Time-Dependent Carrier Flow in a Transistor Structure Under Nonisothermal Conditions" (p 1297-1304)
	IEEE	1979	Chenming Hu: "A Parametric Study of Power MOSFETS" (p 988-998)
✓	IEEE	1979	J.A. Appel, H.M.J. Vaes: "High Voltage Thin Layer Devices (Resurf Devices)" (p 1384-1387)

EXAMINER

Jenm Bralas

DATE CONSIDERED

8/29/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609: Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-449  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b> (Use several sheets if necessary)				Docket Number (Optional)  068758.0102	Application Number  09/780,022  10/633,044	
				Applicant Deboy et al.		
				Filing Date 04/22/99	Group Art Unit: Group Art Unit:	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
<i>Rp</i>	4,914,058	04/03/90	Blanchard	437	203	12/29/87
	4,926,226	05/15/90	Heremans et al.	357	27	09/06/88
	4,941,026	07/10/90	Temple	357	23.4	08/26/88
	4,974,059	11/27/90	Kinzer	357	23.4	08/28/89
	4,975,782	12/04/90	Bauer	357	38	02/22/89
	4,994,871	02/19/91	Chang et al.	357	23.4	12/02/88
	5,008,725	04/16/91	Lidow et al.	357	23.4	12/23/88
	5,010,025	04/23/91	Solomon	437	29	04/03/89
	5,019,522	05/28/91	Meycr et al.	437	29	01/02/90
	5,045,903	09/03/91	Meyer et al.	357	23.4	11/16/89
	5,072,269	12/10/91	Hcida	357	23.6	03/15/89
	5,089,434	02/18/92	Hollinsen	437	41	01/22/90
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO
	WO99/36961	22.07.99	PCT	H01L	23/48	<input type="checkbox"/> x
	DE 197 36 981C2	25.8.97	Germany	H01L	29/78	<input type="checkbox"/> x
	EP 0 939 446 A1	01/09/99	EPO	H01L	29/08	<input type="checkbox"/> x
	WO 00/14807	16.03.00	PCT	H01L	29/78	<input type="checkbox"/> x
	DE 198 40 032 C1	2.9.98	Germany	H01L	29/78	<input type="checkbox"/> x
	WO 99/62123	02.12.99	PCT	H01L	29/861	<input type="checkbox"/> x
	DE 198 23 944 A1	28.5.98	Germany	H01L	29/861	<input type="checkbox"/> x
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)						
	IEEE	1979	Adrian Rusu, Constantin Bulucea: "Deep-Depletion Breakdown Voltage of Silicon-Dioxide/Silicon MOS Capacitors" v (p 201-205)			
	IEEE	1979	Chenming Hu article, "Optimum Doping Profile for Minimum Ohmic Resistance and High-Breakdown Voltage"			
EXAMINER <i>Heinz Krahe</i>				DATE CONSIDERED <i>8/20/04</i>		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609: Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						

Form PTO-1440 OCT 2003 PATENT & TRADEMARK OFFICE NOV 06 2003		DocId Number (Optional) 068758.0102	Application Number 09786,022 10/633,044
INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)		Applicant Deboy et al.	
		Filing Date 04/22/99	Group Art Unit:

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE	
PR	5,126,807	06/30/92	Baba et al.	357	23.4	06/12/91	
	5,182,234	01/26/93	Meyer	437	233	07/26/91	
	5,216,275	06/1/93	cHEN	257	493	09/17/91	
	5,231,474	07/27/93	Hollinger	257	355	07/17/92	
	5,283,201	02/01/94	Tsang et al.	437	31	08/07/92	
	5,340,315	07/04/95	Rumennik	257	331	10/11/94	
	5,438,215	08/01/95	Tihyani	257	401	03/25/94	
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation	
	WO 00/02250	13.01.00	PCT	H01L	29/10	YES	NO
	EP 0 973 203 A2	19.01.00	EPO	H01L	29/06		x
	DE 198 30 332 A1	7.7.98	Germany	H01L	29/06		x

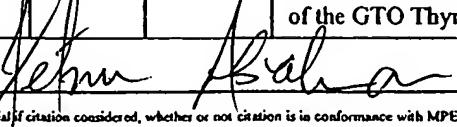
## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

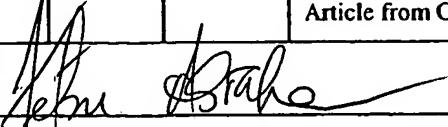
		1979	IEDM Technical Digest excerpt (p. 239, 241)
IEEE		1980	S.C. Sun, James D. Plummer: "Modeling of the On-Resistance of LDMOS, VDMOS, and VMOS Power Transistors" (p 356-357)
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Springer Verlag		1980	Tihanyi, "A Qualitative Study of the DC performance of SIPMOS Transistors"
IEEE		1980	Victor K. Temple, Robert P. Love, Peter V. Gray: "A 600-Volt MOSFET Designed for Low On-Resistance" (p 343-349)
IEEE		1980	William A. Lane, C. Andre T. Salama: "Epitaxial VVMOS Power Transistors" (p 349-355)
IEEE		1980	Takeaki Okabe, Isao Yoshida, Skikayuki Ochi: "A Complementary Pair of Planar-Power MOSFETs" (p 334-339)
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UMI	December 1981		Richard A. Blanchard: "Optimization of Discrete High Power MOS Transistors"

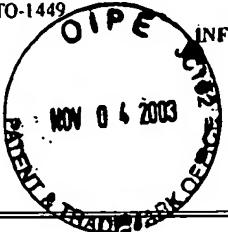
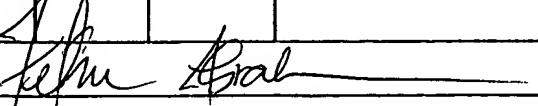
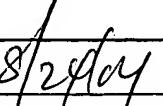
EXAMINER

DATE CONSIDERED

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Form PTO-1449  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b> (Use several sheets if necessary)				DocId Number (Optional) 068758.0102	Application Number 09/786,022 10/633,044	
				Applicant Deboy et al.		
				Filing Date 04/22/99	Group Art Unit: Group 1	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
	5,473,180	12/05/95	Ludikhuize	257	336	07/11/94
	5,559,353	09/24/96	Risch et al.	257	334	11/01/94
	5,648,283	07/15/97	Tsang et al.	437	40	01/31/94
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	5,801,417	09/01/98	Tsang et al.	257	333	08/13/93
	5,883,411	03/16/99	Ueda et al.	257	331	11/23/92
	5,973,360	10/26/99	Tihanyi	257	330	09/21/98
	6,037,631	03/14/00	Deboy et al.	257	339	09/18/98
	US2001/0053568		Deboy et al.	438	138	03/26/01
	US2001/0050549		Deboy et al.	323	313	03/12/01
DOCUMENT NUMBER	DATE	COUNTRY		CLASS	SUB- CLASS	Translation _____
						YES NO
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)						
	IEEE	1981	J.P. Stengl, H. Strack, J. Tihanyi: "Power MOS Transistors for 1000 V Blocking Voltage" (p 422-425)			
	IEEE	1981	Sel Colak: "Effects of Drift Region Parameters on the same properties of Power LDMOST" (p 1455-1466)			
	IEEE	1982	Min-hwa Chi, Chenming Hu: "Some Issues of Power MOSFETS" (p 392-393)			
	IEEE	1982	Chen and Hu article, "Optimum Doping Profile of Power MOSFET Epitaxial Layer"			
	IEEE	1983	P.L. Hower, T.M.S. Heng, C. Huang: "Optimum Design of Power MOSFETS" (p 980-984)			
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	IEEE	1984	Board, Kenneth: "The Optimization of On-Resistance in Vertical DMOS Power Devices with Linear and Hexagonal Surface Geometries"			
		June 1984	B.J. Baliga, M.S. Adler, R.P. Love et al: "Insulated Gate Transistor: A New Three-Terminal MOS-Controlled Bipolar Power Device" (excerpt) (p 1394-1402)			
	IEEE	1984	Akio Nakagawa, David H. Navon: "A Time- and Temperature-Dependent 2-D Simulation of the GTO Thyristor Turn-Off Process" (p 1156-1163)			
EXAMINER				DATE CONSIDERED 8/24/04		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						

Form PTO-1440  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b> (Use several sheets if necessary)				Docket Number (Optional) 068758.0102	Application Number 09/781,022 10/633,044	
				Applicant Deboy et al.		
				Filing Date 04/22/99	Group Art Unit:	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES NO
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)						
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	IEEE	1985	R. Stengl, U. Gösele: "Variation of Lateral Doping—A New Concept to Avoid High Voltage Breakdown of Planar Junctions" (p 154-157)			
		November 1985	C. Frank Wheatley Jr., Gary M. Dolny: "COMFET—The Ultimate Power Device; A General Study of Power Devices" (p 121-128)			
	Academic Press	1986	B. Jayant Baliga: "Epitaxial Silicon Technology"			
			Article from Acta Electronica Sinica, March 1986, "A Novel InGaAs Phototransistor by CaO Emitter" (in Chinese) (p 35-39)			
	IEEE	1986	Jerry G. Fossum, Robert J. McDonald: "Charge Control Analysis of the COMFET Turn-Off Transient" (p 1377-1382)			
	IEEE	1987	X.B. Chen, Z.Q. Song, Z.J. Li: "Optimization of the Drift Region of Power MOSFET's with Lateral Structures and Deep Junctions" (p 2344-2350)			
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	IEEE	April 1987	Daisuke Ueda, Hiromitsu Takagi, Gota Kano: An Ultra-Low On-Resistance Power MOSFET Fabricated by Using a Fully Self-Aligned Process			
	IEEE	1987	Wirojana Tantraporn, Victor A.K. Temple: "Multiple-Zone Single-Mask Junction Termination Extension—A High-Yield Near-Ideal Breakdown Voltage Technology" (p 220-2210)			
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		May 1988	Chen Xingbi, Li Zhaoji, Jiang Xu: "Two-Dimensional Numerical Analysis of High-voltage Semiconductor Electric Fields"			
			Article from Chinese Journal of Semiconductors, May 1988 (p 255-260)			
EXAMINER				DATE CONSIDERED 8/24/04		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						

Form PTO-1449  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b> (Use several sheets if necessary)				Document Number (Optional) 068758.0102	Application Number 09/786,022 10633,044	
				Applicant Deboy et al.		
				Filing Date 04/22/99	Group Art Unit: Group 1	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES NO
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)						
PH	IEEE	Oct. 1988	Zahir Parpia, C. Andre T. Salama, Robert A. Hadaway, "A CMOS-Compatible High-Voltage IC Process" (p 1687-1694)			
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	Solid State Electronics	1990	H.R. Chang, F.W. Holroyd: "High Voltage Power MOSFET's with a Trench-Gate Structure" (p 381-387)			
	Chinese Journal of Semiconductors	1990	Li Zhaoji, Yu Hongquan, Chen Xingbi: "Temperature Distribution of Full Thermal Path of VDMOS" (p 435-440)			
		1991	Article by Xing-Bi Chen presented at 2 <sup>nd</sup> German-Chinese Electronics Week Congress, Shanghai, China.			
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		1998	X.B. Chen et al., "Theory of a novel voltage-sustaining layer for power devices" (from Microelectronics Journal)			
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		May 1998	Article, "Siemens' new MOSFET design drastically cuts on-state resistance"			
	Chinese Journal of Semiconductors	July 1998	Chen article, "Theory of a Novel Voltage Sustaining (CB) Layer for Power Devices" (from Chinese Journal of Electronics)			
		July 1998	Steve Bush, "Five-fold resistance cut for high-voltage FETs"			
EXAMINER 				DATE CONSIDERED 		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						

<p>Form PTO-149 U.S. PATENT &amp; TRADEMARK OFFICE NOV 06 2003 INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)</p>				Docto Number (Optional) 068758.0102	Application Number 6978022 107633844	
				Applicant Debay et al.		
				Filing Date 04/22/99	Group Art Unit:	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES NO
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)						
		1998	Lorenz et al. article, "Improved MOSFET An Important Milestone Toward a New Power MOSFET Generation" featured in PCIM			
		1999	X.B. Chen et al. "High voltage sustaining structure with embedded oppositely doped regions"			
			Lai, et al.; "Characteristics and Utilization of a New Class of Low On-Resistance MOS-Gated Power Device" (1999)			
		July 1999	Article "Power Semiconductors Proliferate" published in Electronics Products magazine re: Infineon CoolMOS products and IR CoolMOS- equivalent devices.			
	Chinese Journal of Semiconductors	July 1999	Xing Bi Chen & Johnny K.O. Sin "A Novel High Voltage Sustaining Structure with Buried Oppositely Doped Regions"			
		June 2000	Chen article, "Optimization of the Specific On-Resistance of the CoolMOS," published by IEEE Transactions on Electron Devices			
EXAMINER <i>John Deah</i>				DATE CONSIDERED <i>8/29/04</i>		
<p>EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.</p>						